Amendments to the Claims

Please amend Claims 1-3, 5, 13-17 and 23. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Currently amended) A data demultiplexer for demultiplexing data from a communication link comprising:

a clock source;

a higher frequency data demultiplexer which demultiplexes the data on the communication link to an intermediate frequency signal, a clock signal from the clock source being precisely distributed to the higher frequency data demultiplexer; and

a lower frequency data demultiplexer ~~directly~~ coupled to the higher frequency demultiplexer which further demultiplexes the intermediate frequency signal, the clock signal being less precisely distributed to the lower frequency data demultiplexer.

2. (Currently amended) A data demultiplexer as claimed in claim 1 wherein the higher frequency data ~~multiplexing stage~~ demultiplexer and the lower frequency data ~~multiplexing stage~~ demultiplexer are formed on a single circuit chip.

3. (Currently amended) A data demultiplexer as claimed in claim 2 wherein the clock signal is frequency divided to clock the lower frequency data ~~multiplexing stage~~ demultiplexor.

4. (Original) A data demultiplexer as claimed in claim 3 wherein the clock signal is frequency divided by a ring counter.

5. (Currently amended) A data demultiplexer as claimed in claim 1 wherein the clock signal is frequency divided to clock the lower frequency data ~~multiplexing stage~~ demultiplexor.

6. (Original) A data-demultiplexer as claimed in claim 5 wherein the clock signal is frequency divided by a ring counter.

7. (Original) A data demultiplexer as claimed in claim 1 in which the higher frequency data multiplexer is clocked by a multiplying delay locked loop bit clock generator.

8. (Original) A data demultiplexer as claimed in claim 1 wherein the data on the communication link comprises a one-bit-wide bitstream.

9. (Original) A data demultiplexer as claimed in claim 8 wherein the intermediate frequency signal is two bits wide.

10 (Original) A data demultiplexer as claimed in claim 1 wherein the intermediate frequency signal comprises more than two parallel bits.

11. (Original) A data demultiplexer as claimed in claim 10 wherein the higher frequency data multiplexer is clocked by an N-phase overlapping clock.

12. (Original) A method of demultiplexing data from a communication link comprising:

demultiplexing the data from the communication link to an intermediate frequency signal using a clock signal precisely distributed from a clock source; and

further demultiplexing the intermediate frequency signal to a lower frequency signal using the clock signal less precisely distributed from the clock source.

13. (Currently amended) A ~~data communication circuit~~ method of demultiplexing as claimed in claim 12 wherein the steps are performed in a higher frequency data multiplexing stage and a lower frequency data multiplexing stage formed on a single circuit chip.

14. (Currently amended) A ~~data communication circuit~~ method of demultiplexing as claimed in claim 13 wherein the clock signal is frequency divided to clock the lower frequency data multiplexing stage.

15. (Currently amended) A ~~data communication circuit~~ method of demultiplexing as claimed in claim 14 wherein the clock signal is frequency divided by a ring counter.

15. (Currently amended) A ~~data communication circuit~~ method of demultiplexing as claimed in claim 14 wherein the clock signal is frequency divided by a ring counter.

16. (Currently amended) A ~~data communication circuit~~ method of demultiplexing as claimed in claim 12 wherein the clock signal is frequency divided to clock the lower frequency data multiplexing stage.

17. (Currently amended) A ~~data communication circuit~~ method of demultiplexing as claimed in claim 16 wherein the clock signal is frequency divided by a ring counter.

18. (Original) A method of demultiplexing as claimed in claim 12 in which the higher frequency data multiplexer is clocked by a multiplying delay locked loop bit clock generator.

19. (Original) A method of demultiplexing as claimed in claim 12 wherein the higher frequency signal on the communication link comprises a one-bit-wide bitstream.

20. (Original) A method of demultiplexing as claimed in claim 19 wherein the intermediate frequency signal is two bits wide.

21. (Original) A method of demultiplexing as claimed in claim 20 wherein the intermediate frequency signal comprises more than two parallel bits.

22. (Original) A method of demultiplexing as claimed in claim 21 wherein the higher frequency data multiplexer is clocked by an N-phase overlapping clock.

23. (Currently amended) A data demultiplexer for demultiplexing data from a communication link comprising:

high frequency data demultiplexer means relying on a clock signal precisely distributed from a clock source for demultiplexing the data on the communication link to an intermediate frequency signal; and

lower frequency data demultiplexer means relying on the clock signal less precisely distributed from the clock source for demultiplexing the intermediate frequency signal.

24. (Original) A data demultiplexer on an electronic chip for demultiplexing data from a communication link comprising:

a higher frequency data demultiplexer on the chip which demultiplexes the data on the communication link to an intermediate frequency signal; and

a lower frequency data demultiplexer on the chip coupled to the higher frequency demultiplexer which further demultiplexes the intermediate frequency signal.